W-Band Flip-Chip Interconnects on Thin-Film Substrate

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Abstract — **A flip-chip approach is presented using a thin-film microstrip line (TFMSL) on silicon as carrier substrate. Thin-film technology allows to employ cheap low-resistivity Si wafers without degrading mm-wave performance. By means of 3D em simulation, an optimized interconnect is designed for the 77 GHz band. Measurements of test structures up to 100 GHz demonstrate the potential of this approach.**

I. MOTIVATION

Cost-effective mounting in the mm-wave frequency range is still an unresolved issue. Among the possible interconnect technologies, flip-chip is the most promising candidate, allowing a fast and easy-to-handle placement of the chips. The small-sized bump dimensions ensure good electrical performance up to 100 GHz and beyond. But several side effects may deteriorate flip-chip characteristics. The most important one is coupling into unwanted substrate modes, which is particularly pronounced when using conductor-backed coplanar waveguide as transmission-line on the motherboard. Also, for conventional ceramic boards, the relatively large dimensions of metalization and via-holes limit the frequency band available.

The thin-film technology offers solutions to these problems. It allows for line structures with cross-sections smaller than those available on ceramic substrates, a precondition for operation in the upper mm-wave frequency range. Thus, thin-film structures can be realized with dimensions comparable to the flip-chip interconnect, which reduces reflections.

The second important advantage in using thin-film is that the typical transmission-line geometry, the thin-film microstrip line (TFMSL), is a surface-oriented line type. The ground conductor shields the TFMS fields against the substrate. This means: the electrical properties of the carrier substrate do not influence the performance. Thus, inexpensive lossy substrates can be used, e.g. low-resistive silicon. On the contrary, the substrate losses are of advantage here because they can be utilized in order to absorb parasitic substrate modes.

A combination of the flip-chip technique with a thin-film motherboard was presented already in [1], treating the lower mm-wave frequency range around 40 GHz. The purpose of this paper is to demonstrate feasibility of this approach for the W band around 77 GHz.

II. THIN-FILM FLIP-CHIP INTERCONNECT

So far, the thin-film approach has been applied mainly for on-chip transmission lines and as a carrier in multi-chip boards with conventional interconnects (wire bonding, embedded chips), see, e.g. [2,3].

The thin-film structure used here consists of two Au metalization layers (ground, signal) and one dielectric layer on top of a low-resistivity silicon wafer. BCB with an $\varepsilon_r = 2.7$ and a nominal thickness of 20 µm forms the dielectric thin-film. Electromagnetic field simulation (finite-difference method in frequency domain, FDFD) was employed to optimize the pads for on-wafer probing. Thin-film microstrip (TFMSL) is used as transmission line. Strip width is about 50 µm for 50 Ω characteristic impedance, the width of the ground metalization was chosen to be 400 µm.

The transition from the TFMSL on the motherboard to the CPW on the flipped chip is shown in Fig. 1. A coplanar GaAs chip is used. The geometry of the in-out cell was optimized by means of 3D em simulation in order to meet the following 3 constraints simultaneously:

(i) Additional pad area to allow for automated on-wafer characterization of the bumped chip before flip-chip bonding.
(ii) Minimum consumption of chip area.
(iii) Low reflection of the entire interconnect after mounting (less than –20 dB per interconnect at 77 GHz).

For the first 2 conditions, only the chip was considered. The third optimization goal requires simulation of the complete interconnect including both chip and thin-film carrier substrate.

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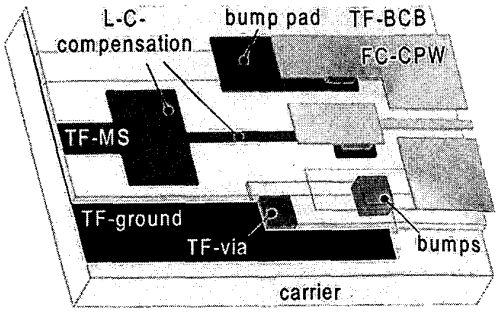

Fig. 1 The flip-chip interconnect on thin-film carrier substrate (GaAs chip substrate not shown).

With these considerations in mind, the interconnect was optimized for minimum reflection around 77 GHz by means of 3D em simulation. We found that a simple pad structure could not meet the specs, so that the transition needs a compensation structure. In order to save on GaAs chip area and to remain compatible with other mounting techniques this compensation section was introduced on the thin-film substrate only.

Another important design criterion is substrate moding. Because the backside of the carrier substrate is conducting one needs to consider the parallel-plate-line-mode (PPL), which is excited at the interconnect and propagates on the chip side between the CPW on the chip surface and the backside metalization of the carrier. On the thin-film side, the PPL mode propagates in the carrier substrate below the TFMSL ground metalization. Since the PPL mode causes crosstalk and reduces isolation, it has to be suppressed as far as possible. At this point, the advantages of using low-resistivity silicon as the carrier become obvious. The Si losses act as absorber increasing attenuation of the PPL mode and thus reducing coupling to other structures.

On the TFMSL side, the PPL fields are entirely within the lossy material, which leads to large attenuation. Below the chip, parts of the PPL fields are outside the Si in the gap between chip and thin-film substrate. Thus, attenuation is smaller but still considerably larger than for non-conducting carrier substrates. Moreover, in our design, we took into account low PPL excitation as a further optimization goal. As a result, the interconnect presented here suppresses the excitation of the PPL mode to less than –20 dB in the interesting frequency range as illustrated by Fig. 2.

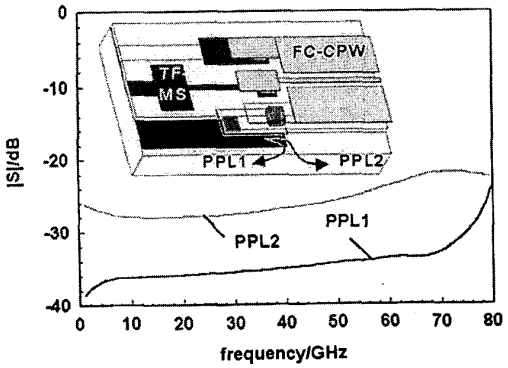

Fig. 2. Coupling to parasitic substrate modes as a function of frequency: transmission from TFMSL mode to PPL1 and PPL2 modes below TFMSL and the chip, respectively (carrier involves metalization on backside, for details see inset).

III. Test Set-up For Verification

In order to verify the design, test structures were fabricated. The GaAs chip contains various passive structures, the most important of which are shown in Fig. 3. They consist of 50 Ω coplanar transmission-lines with the optimized in-out cells described above. Beside the simple thru-line a second version including two additional flip-chip interconnects are realized in order to emphasize the parasitics of the transitions in the measurements (see lower line in Fig. 3). Fig. 3 illustrates the complete back-to-back set-up for on-wafer characterization. The total length of each line system is about 9 mm.

Flip-chip bonding was performed by thermocompression using two types of bumps with 30 µm and 50 µm diameter and a designed height of 30 µm after bonding.

To ensure that for comparison reasons the electrical parameters can be extracted and defined from measurements properly, further test structures were designed and processed on the same thin-film wafer. This comprises a series of TFMSLs with different lengths as well as chains of prober pads positioned face-to-face. Also, a collection of capacitors and resonators of different size were fabricated in order to obtain separate information about the dielectric constant and the thickness of the thin-film.

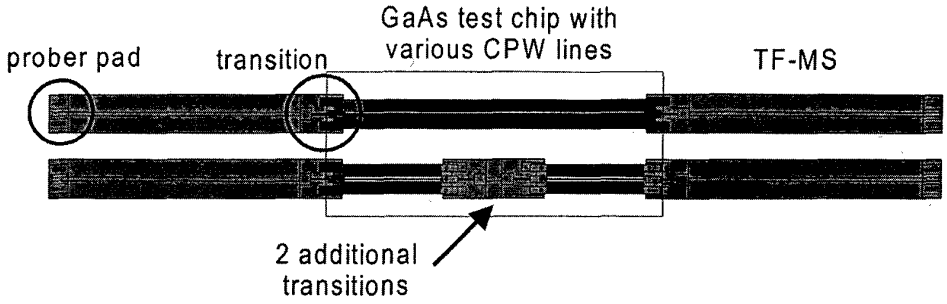

Fig. 3. The test structures with pads for on-wafer probing and flip-chip transitions (both chip and thin-film layouts are shown):
- CPW through-line (length 3106 µm).
- CPW through-line with 2 additional transitions and intermediate TFMSL section (each CPW is 1000 µm long).

III. Results

From measurements of the thin-film test structures the actual behavior of the CPW prober pads as well as the line properties of the TFMS were extracted. The results indicated that the thickness of the thin-film is about 17 µm. This influences impedance of the TFMSL and the interconnect behavior. Also, the CPW structures on the GaAs chip were measured before bonding. This allows one to remove the pad and transmission-line characteristics from the measurements and fit an equivalent-circuit description. Additionally, REM pictures were taken in order to check the actual dimensions of the fabricated samples. Fig. 4 shows the cross-section of the bump region.

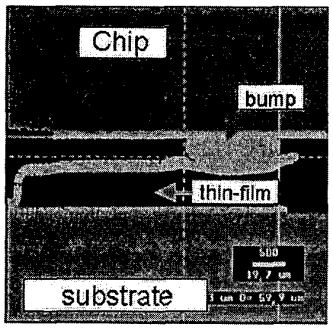

Fig. 4. Photograph of a longitudinal cut through TF ground pad with via, bump, and chip.

Measurements of the thru-line structures of Fig. 3 are presented in Figs. 5 and 6. In both cases, one clearly observes a reflection minimum in the frequency range between 70 and 90 GHz, which was intended by the design.

Minimum return loss in this range is 16 dB for the back-to-back structure, which relates to more than 20 dB for the single transition. This is supported by the data for the structure with 2 additional interconnects (Fig. 6), which shows only slightly higher reflections than for the standard case of Fig. 5. Thus, one can state that the specs are met.

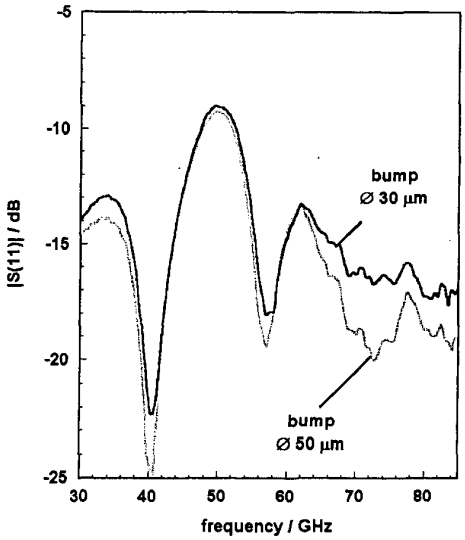

Fig. 5. Input reflections against frequency for the upper line system in Fig. 3 (measurements of back-to-back structure with 2 interconnects, bumps with 30µm and 50µm nominal diameter).

Comparing the two nominal bump diameters of 30μm and 50μm one finds only small deviations, with advantages for the larger bumps, particularly pronounced for the 4-interconnect structure (Fig. 5). Since pad size and bump heights are the same, however, the resulting changes remain small. This is advantageous because bump diameter is a parameter difficult to control.

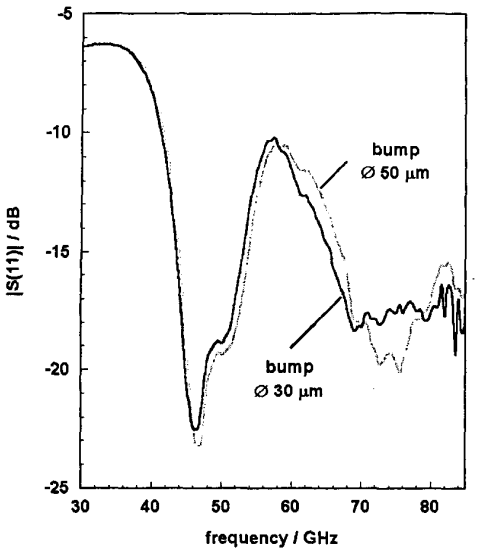

Fig. 6 Input reflections against frequency for the lower line system in Fig. 3 (measurements of back-to-back structure with 4 interconnects, bumps with 30μm and 50μm nominal diameter).

Going into the details, it is interesting to have a look into the characteristics of a single transition, which is difficult to extract from the back-to-back case in Figs. 5 and 6. Therefore, the em simulation results (FDFD) for a single transition are plotted in Fig. 7. Two sets of input parameters are treated, the nominal design values and a worst-case constellation based on the fabrication tolerances observed. As can be seen, the designed minimum at 77 GHz is shifted to higher frequencies and the overall reflection increases. Hence, yield centering is important for a successful design.

Summarizing, the measurements clearly prove feasibility of this flip-chip approach in the W-band frequency regime.

II. Conclusions

A flip-chip mounting scheme on thin-film motherboard for W-band applications is presented. The in-out cell on the coplanar GaAs chip is optimized to allow on-wafer probing of the bumped chip. Suppression of substrate moding due to the PPL mode is included in the design and enhanced by using thin-film microstrip on low-resistivity silicon for the carrier substrate. Test structures were fabricated and measured. The results demonstrate the potential of the new approach, yielding reflections below -16 dB for the back-to-back structure with 2 and 4 interconnects in the frequency range from 70 to 90 GHz. The simulations point out the importance of fabrication tolerances and yield-centering in the design.

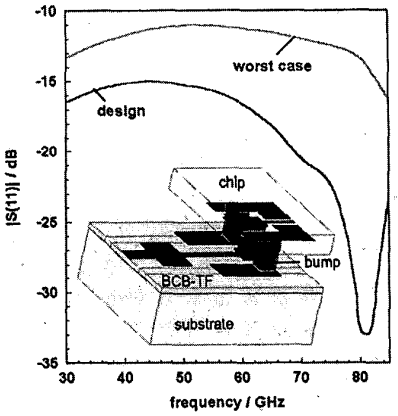

Fig. 7 Input reflections of a single flip-chip interconnect as a function of frequency: em simulation with nominal dimensions ("design") and worst case constellation considering fabrication tolerances ("worst case").

Acknowledgement

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